

P6050 / P6060 PCB Mount Pressure Sensors with Analog or Digital Output



Description

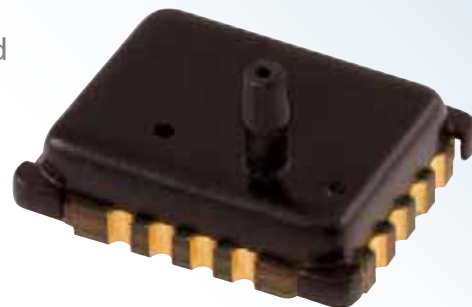
The P6050/P6060 series pressure sensors incorporate a piezo-resistive sense element in a low profile, surface mount package.

Using a 5V input, the sensors provide a 0.5 to 4.5 Vdc output proportional to pressure. The sensor can optionally provide a digital output conforming to SPI protocol.

Internal temperature compensation using a state-of-the-art ASIC provides an accurate, easy to use device.

Features

- Rugged, Low Profile Package
- Amplified, Temperature Compensated Linear Output or Digital SPI Output
- Internal 10bit A/D Converter
- EMI/RFI & ESD Protected
- Enhanced Accuracy Option (P6060)
- Custom Pressure Ranges and Port Configurations



Applications

- Medical
 - Oxygen Concentrators
 - Respirators
 - Sleep Apnea
 - Hospital Beds
- Industrial
 - Instrumentation
 - Pneumatic Controls
 - Robotics

Standard Full Scale Pressure Ranges

- 13" H₂O
- 0-1, 2.5, 15, 20, 50, 75 PSIA, PSIG and PSID

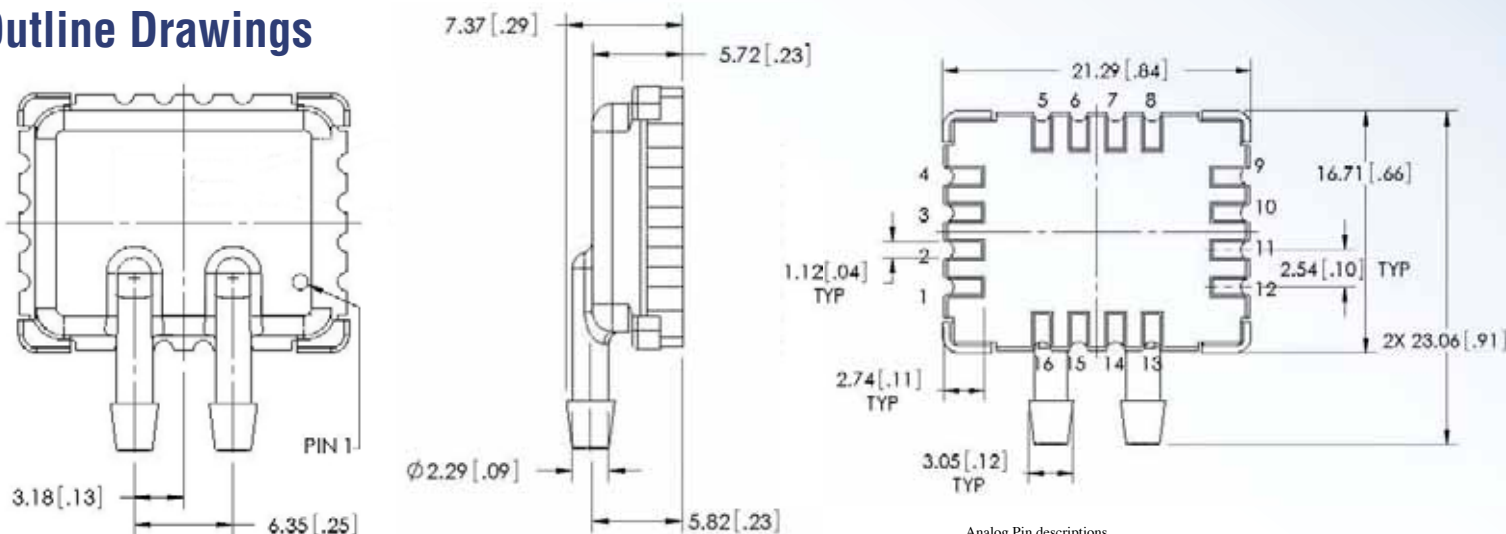
Technical Specifications

Note: Performance Specifications with 5v ± 0.002 Vdc supply at 25°C

| | | | |
|-----------------------------------|---|-------------------------------------|---|
| Pressure Ranges: | 13" H ₂ O 0-1, 2.5, 15, 20, 50, 75 PSIA, PSIG and PSID | Storage Temperature: | -40°C to + 125°C |
| Proof Pressure: | 2X Max. Pressure | Service Life: | 10,000,000 Cycles Min. |
| Burst Pressure: | 3X Max. Pressure | Vibration: | 10 G from 20 Hz to 2000 Hz |
| Supply Voltage: | 5.0 ± 0.25 Vdc | Shock: | 50G ½ Sine Wave |
| Supply Current: | 4mA Max. | Humidity: | 95% RH, Non-Condensing |
| Linearity Error: | ±0.5% of Full Span Max. | Weight: | 1.3 Grams Max. |
| Response Time: | 10ms Max to 63% of F.S. Pressure with Step Change on Input | Output Options: | Analog (Ratiometric) 0.5 to 4.5 Vdc Digital – Slave SPI Protocol |
| Voltage: | | - Option A | Position Insensitive |
| Ratiometricity: | ±1.5% of Span Max. | - Option D | H) Horizontal, (V) Vertical, D) Dual Horizontal |
| Total Error Band: (0 to 60°C): | ±2% of Span Max. (P6050) ±1% of Span Max. (P6060) | Preferred Mounting Position: | Barb for 3/16 ID Tubing |
| Output Impedance: | < 100 Ω | Pressure Connection: | |
| Operating Temperature: | -20°C to + 85°C | Recommended Interface Impedance: | Min. Load 25 kΩ |
| | | Over-Voltage Protection: | 16Vdc |
| | | Reverse Polarity Protection: | -6 Vdc |

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Outline Drawings



How to Order

Please contact factory for other port configurations.

A typical order number has three codes, separated by two hyphens. Standard seal material is silicone. Standard pressure connection is barbed tube fitting

P6050/P6060 Miniature Pressure Sensors

Pressure Range

| | |
|----|---|
| 13 | 0-13" H ₂ O (G) Gage, (D) Differential |
| 1 | 0-1 PSI (G) Gage, (A) Absolute or (D) Differential |
| 2 | 0-2 PSI (G) Gage, (A) Absolute or (D) Differential |
| 5 | 0-5 PSI (G) Gage, (A) Absolute or (D) Differential |
| 15 | 0-15 PSI (G) Gage, (A) Absolute or (D) Differential |
| 20 | 0-20 PSI (G) Gage, (A) Absolute or (D) Differential |
| 50 | 0-50 PSI (G) Gage, (A) Absolute or (D) Differential |
| 75 | 0-75 PSI (G) Gage, (A) Absolute or (D) Differential |

Output

| | |
|---|-----------------------|
| A | Analog Voltage Output |
| D | Digital SPI Output |

Pressure Port Configuration

| | |
|---|--|
| H | Horizontal Pressure Port |
| V | Vertical Pressure Port |
| D | Dual Horizontal (Differential) Pressure Port |

P6050 15 A - A - D

Example: P6050-15A-A-D

*** For high accuracy version specify P6060 vs. P6050**

Example: P60610 - 15A - A - D

Contact Kavlico for accuracy options, custom packaging, alternative pressure ranges, or other OEM or application specific requirements.

Analog Pin descriptions

| Pin # | Description |
|-------|-------------|
| 2 | VS |
| 3 | GND |
| 4 | Vout |

All remaining pins are No Connection

Digital Pin descriptions

| Pin # | Description |
|-------|--------------|
| 6 | GND |
| 8 | SCK |
| 13 | MISO/ Output |
| 14 | DRDY |
| 15 | SS |
| 16 | VS |

All remaining pins are No Connection

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P6050 Digital SPT Interface

The P6050 is capable of generating a digital output signal in SPI format. In this configuration external pressure is measured and temperature compensated as in the analog output configuration.

The calibrated, temperature compensated analog signal corresponding to pressure is internally routed to a 10 bit analog to digital converter and then output as a digital signal conforming to a SPI interface protocol. This P6050 output can be tied directly to a microprocessor along with the control pins without requiring any additional circuitry or processing.

PIN Description

| | |
|------|--|
| SS | Slave Select |
| MISO | Master-In, Slave-Out (P6050 Output pin) |
| SCK | Serial clock (always driven by the master) |
| DRDY | Data Ready (Generated by the P6050) |

Implementation

An internal initialization procedure performs the necessary operations to configure the SPI port as a slave port upon power up. When the initialization is complete, the sensor enters into a standby state waiting for the SS line to be brought low. During this period, the pressure sensor still internally tracks pressure but no data is output on the device pins. The unit must be protected from overpressure conditions regardless of the state of the outputs. The sensor detects that the SS line has gone low and internally processes the pressure information. At the end of the processing, 24 bits of data are output on the MISO line responding to the 24 clock pulses from the master. Among the 24 bits of data, 10 bits of left justified measurement results are shifted out in 2 eight bit bytes with the last 6 bits of the second byte unused information. The third byte is checksum data.

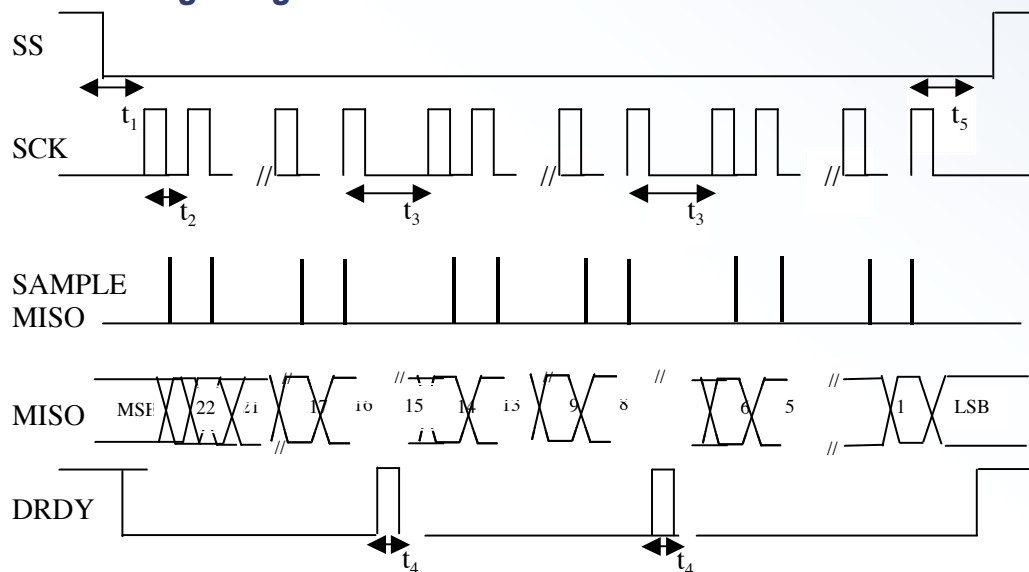
Theory of Operation

All accesses from the P6050 module are through a hardware handshaking, serial peripheral interface (SPI). The interface consists of 4 signals: SS, SCK, MISO and DRDY. The P6050 module is configured as a slave device. The SS line must be low prior to a data transfer and must stay low during the entire transfer. The P6050 begins the pressure measurement procedure after the SS line is brought low. The DRDY line is initially high. At the end of the measurement, the DRDY line is set to low by the P6050 and 24 bits of data are shifted out from the device on the MISO line with the MSB shifted first. The bits are shifted out in response to 24 CLK pulses in groups of three 8 clock pulses @ 250 KHz. The first 8 bits are shifted out and DRDY goes high for 12us while the second byte is processed. When DRDY is set low by the P6050, the second byte is available to be shifted out. Likewise, after the second byte, DRDY goes high for 12us while the checksum byte is generated. When DRDY goes low, the last byte of data can be shifted out. The clock polarity used with the P6050 must be normally low with valid data presented on the high state of the clock. The DRDY line should always be used to insure that the data is clocked out on the MISO line only when valid data is available. It is the device master's responsibility to give the P6050 enough time to prepare its next data transmission before starting a new transfer.



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SPI Timing Diagram



DC Characteristics

Applicable over the recommended operating range of 0C to 60C, $V_{CC}=5V \pm .25V$

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|----------|---------------------|---|-------------|------|--------------|---------|
| V_{CC} | Supply Voltage | | 4.75 | 5.0 | 5.25 | V |
| I_{CC} | Supply Current | $V_{CC}=5.0$ | | 10 | 15 | mA |
| I_{SS} | Standby Current | | | 10 | 15 | mA |
| I_{IL} | Input leakage | $V_{IN}=0V$ to V_{CC} | | <.05 | 1 | μA |
| I_{OL} | Output Leakage | $V_{IN}=0V$ to V_{CC} | | 10 | | μA |
| V_{IL} | Input Low Voltage | | -0.5 | | $0.3V_{CC}$ | V |
| V_{IH} | Input high Voltage | | $0.6V_{CC}$ | | $V_{CC}+0.5$ | V |
| V_{OL} | Output Low Voltage | | | | .6 | V |
| V_{OH} | Output High Voltage | $V_{CC}=5.0, I_{OL} = .15ma$ $I_{OH} = -100ua$ | 4.3 | | | V |

AC Characteristics

Applicable over the recommended operating range of 0C to 60C, $V_{CC}=5V \pm .25V$

| Symbol | Parameter | Min | Typ | Max | Units |
|-------------|-------------------------------------|-----|-----|------|---------|
| f_{SCK} | SCK Clock Frequency | 1 | 10 | 250 | KHz |
| t_2 | SCK period | 4 | 100 | 1000 | μS |
| t_{RI} | Input Rise Time | | | 2 | ns |
| t_{RF} | Input fall time | | | 2 | ns |
| t_{WH} | SCK High Time | 2 | | | μs |
| t_{WL} | SCK Low Time | 2 | | | μs |
| t_1 | SS assertion to first SCK edge | 110 | | | μS |
| t_3 | SCK set up time | 12 | | | μS |
| t_4 | DRDY busy | 2.8 | | | μS |
| t_5 | Last SCK edge to de-assertion | 4 | | | μS |
| t_{setup} | Data valid setup time from SCK rise | 125 | | | ns |
| t_{hold} | Data hold time | 2 | | | μs |

